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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/929,765	08/14/2001	Chih Chin Liao	56370	9374

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/929,765	LIAO, CHIH CHIN	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,8,11 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,8,11 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Arguments filed on March 12, 2007.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Prior Art Figures 3 and 4 (APAF) in view of Takahama (JP 6-157238).

In re claim 6, the APAF 3 and 4 shows a BGA package comprising: a substrate 10 having a front and back side, a chip 20 mounted on the front side of the substrate, the chip having an array of bond pads 30B, an array of solder balls 40 on the back side of the substrate, and an array of bond fingers (60A-60D) beside the chip and electrically connected to the bond pads of that chip by a plurality of first bonding wires (50B). An array of electrically conductive vias (80) penetrate from the front to the back side of the substrate and connect to the solder balls. The package also comprises a plurality of continuous electrically-conductive traces (70A-70D) for connecting a first subgroup of the bond fingers to corresponding ones of the vias. The continuous traces including at least one trace interposed between a second subgroup (60B) of the bond fingers and their corresponding vias. The APAF shows all of the elements of the claims except the single layer substrate and the electrically conductive bridge. Takahama shows (fig. 3

and abstract) shows a semiconductor device comprising a single layer substrate (21) having traces (3, 4, and 5) and a conductive bridge (8) in the form of a bond wire spanning in an overhead manner across the traces. The bond wire is free of the interposing traces and has an unfilled gap between the wire and traces. When combined with the APAF, the second bonding wire as a bridge would be free of interference with the first bonding wire since it would not be beneficial for any wires to touch or interfere with each other and thus causing a short circuit. With this configuration, the density of wiring can be increased ultimately increasing the level of integration of the device. When combined with the APAF, the top position of the conductive bridge as a second bonding wire is lower in height than a top position of the first bonding wires. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the connections of the APAF by forming conductive bridges spanning over traces as taught by Takahama to increase the wiring density and ultimately improve the integration of the semiconductor device.

In re claim 14, when the APAF 3 and Takahama are combined the bonding wire of Takahama has one end electrically connected by a first trace to the corresponding via (80A) of the APAF 3, and the other end electrically connected by a second trace to the corresponding bond finger (60B) of the APAF 3.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Figures 3 and 4 (APAF) in view of Takahama (JP 6-157238) as applied to claim 6 above, and further in view of Abrams (US 3,560,256).

In re claim 8, the APAF and Takahama show all of the elements of the claims except the bond wire made of gold. Abrams discloses a bridge/crossover that is made of gold wires or includes a resistor (col. 4, lines 3-6, & 25-31) and is free of interference with the electrically conductive trace due to the insulating material (27) between the bridge and traces. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the APAF and Takahama by employing gold conductive bridge structures that cross over circuit traces as taught by Abrams to suitably increase the packing density of the circuit.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Prior Art Figures 3 and 4 (APAF) in view of Takahama (JP 6-157238) and Abrams (US 3,560,256)

In re claim 11, the APAF 3 and 4 shows a BGA package comprising: a substrate 10 having a front and back side, a chip 20 mounted on the front side of the substrate, the chip having an array of bond pads 30B, an array of solder balls 40 on the back side of the substrate, and an array of bond fingers (60A-60D) beside the chip and electrically connected to the bond pads of that chip. An array of electrically conductive vias (80) penetrate from the front to the back side of the substrate and connect to the solder balls. The package also comprises a plurality of continuous electrically-conductive traces (70A-70D) for connecting a first subgroup of the bond fingers to corresponding ones of the vias. The continuous traces including at least one trace interposed between a second subgroup (60B) of the bond fingers and their corresponding vias. The APAF

shows all of the elements of the claims except the electrically conductive bridge as a zero resistance chip resistor. Takahama shows (fig. 3 and abstract) shows a semiconductor device comprising a single layer substrate (21) having traces (3, 4, and 5) and a conductive bridge (8) in the form of a bond wire spanning in an overhead manner across the traces. The bond wire is free of the interposing traces and has an unfilled gap between the wire and traces. With this configuration, the density of wiring can be increased ultimately increasing the level of integration of the device. When combined with the APAF, the top position of the conductive bridge as a second bonding wire is lower in height than a top position of the first bonding wires. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the connections of the APAF by forming conductive bridges spanning over traces as taught by Takahama to increase the wiring density and ultimately improve the integration of the semiconductor device.

Neither reference shows that the conductive bridge is a zero resistance chip resistor. Abrams shows (fig. 1) a circuit in which crossover or conductive bridges are used to increase the packing density of the circuit (col. 2, lines 14-26). The electrically conductive bridge 26 spans in an overhead manner across interposing traces (22c & 22d) and connect one end of a trace 22b to the end of another trace 22a. There is a gap between the bridge and the interposing trace (that gap is filled with an insulating material). The bridge/crossover is made of gold wires or includes a resistor (col. 4, lines 3-6, & 25-31) and is free of interference with the electrically conductive trace due to the insulating material (27) between the bridge and traces. Abrams does not specifically

mention that the chip resistor has zero resistance. However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to set the resistance to any desired value, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the APAF and Takahama by employing conductive bridge structures such as chip resistors that cross over circuit traces as taught by Abrams to also increase the packing density of the circuit.

Response to Arguments

Applicant's arguments with respect to claims 6, 8, 11, and 14 have been considered but are moot in view of the new ground(s) of rejection. See the new rejection above concerning the rejection of the claims over APAF 3 and 4.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew E. Warren
May 23, 2007